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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,108	07/15/2003	Marcus Janke	S&ZIO020101	8615

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EXAMINER
DAVIS, ZACHARY A

ART UNIT	PAPER NUMBER
2137	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/620,108	JANKE, MARCUS
	Examiner	**Art Unit**	
	Zachary A. Davis	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>12 February 2008</u>.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-17</u> is/are pending in the application.
     4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1-17</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
     a) ☐ All   b) ☐ Some * c) ☐ None of:
         1. ☐ Certified copies of the priority documents have been received.
         2. ☐ Certified copies of the priority documents have been received in Application No. _____.
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)   Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)   Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15

January 2008 has been entered.

2.   By the above submission, Claims 1, 2, 6-9, and 11-17 have been amended. No

claims have been added or canceled. Claims 1-17 are currently pending in the present

response.

Response to Arguments

3.   Applicant's arguments with respect to claims 1-17 have been considered but are

moot in view of the new ground(s) of rejection.

Specification

4.   Applicant is thanked for the attention to detail in correcting the various errors

throughout the specification, particularly those not specifically pointed out in previous

Office actions. The Examiner notes that the amendment appears to have introduced an

additional error, as detailed below.

5.   The disclosure is objected to because of the following informalities:

        The specification appears to contain grammatical errors. Specifically, in the

amendment at page 5 of the present response, the sentence that has been amended to

read "Each communication operation between the terminal and the security module

during one and the same communication operation with the security module, being

designated to send at least the part of algorithm code or the complete algorithm code to

the volatile memory of the security module." is now a fragment (in particular, there is not

a clear verb).

        Appropriate correction is required. Applicant is thanked for correction of the

errors in the specification, and Applicant's cooperation is again requested in correcting

any additional errors of which Applicant may subsequently become aware in the

specification.

Claim Objections

6.   The objections to Claims 1, 11, 13-15, and 17 for informalities are withdrawn in

light of the amendments to the claims.

Claim Rejections - 35 USC § 112

7.   The rejection of Claims 6, 7, 9, and 11-17 under 35 U.S.C. 112, second

paragraph, as indefinite is withdrawn in light of the amendments to the claims.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

9.   Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Schneier et al, US Patent 5768382, in view of Obana et al, JP11338993 (cited on the

information disclosure statement received 20 July 2005; an variant translation is

provided herewith, although the translation provided by Applicant has also been

considered).

In reference to Claim 1, Schneier discloses a security module (column 11, lines 34-44; column 7, lines 38-41; column 12, lines 6-44) including a data interface that includes algorithm code concerning a processing of secrets (column 14, lines 19-21); an interface for receiving power (Figure 4D, power 27); a volatile memory storing the received algorithm code, where the volatile memory is cleared when the power supply is interrupted (Figure 4D, volatile memory 23b; column 14, lines 22-26); and a processor for performing the algorithm code (Figure 4C, CPU 302; column 11, lines 55-57). However, Schneier does not explicitly disclose a power interface for receiving power supplied externally from a terminal.

Obana discloses a security module (Figure 2, IC card 100) including a data interface that receives algorithm code concerning a processing of secrets (Figure 2, I/O 220; paragraph 0017); an interface for receiving power (Figure 2, I/O interface 220; paragraph 0017, where a current supply to the IC card is mentioned); a memory storing the algorithm code, where the memory can be cleared (Figure 2, RAM 250; paragraphs 0017 and 0037); and a processor that performs the algorithm code to determine a result (Figure 2, CPU 210; paragraph). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the security module of Schneier to have an interface for an external supply of power, in order to increase portability by providing the predictable result of allowing a power supply to be used that is not within the module itself, while still allowing the memory to be cleared when the power supply is interrupted (see Obana, paragraph 0037).

In reference to Claim 2, Schneier and Obana further disclose non-volatile memory storing a remainder of algorithm code (Schneier, column 14, lines 17-19; Obana, Figure 2, ROM 230 or EEPROM 240; paragraph 0036).

In reference to Claim 3, Schneier and Obana further disclose means for performing authentication (Schneier, column 20, lines 15-26).

In reference to Claim 4, Schneier and Obana further disclose receiving a certificate and examining a certificate, and decrypting code (Schneier, column 14, lines 17-26; column 44, lines 30-35; column 50, lines 36-37; Obana, paragraphs 0017-0022).

In reference to Claims 5 and 8, Schneier and Obana further disclose a memory managing unit and code that includes addresses (Schneier, column 7, lines 48-61; Obana, paragraph 0031).

In reference to Claim 6, Schneier and Obana further disclose means for monitoring a predetermined security condition and clearing the volatile memory if the condition is fulfilled (Schneier, column 14, lines 19-26; Obana, paragraphs 0017 and 0037).

In reference to Claim 7, Schneier and Obana further disclose that the algorithm code can perform a symmetric cryptographic algorithm such as DES or an asymmetric cryptographic algorithm such as RSA (see Schneier, column 9, line 58-column 10, line 11, and column 10, lines 27-40).

In reference to Claim 9, Schneier and Obana further disclose updating the code (Schneier, column 14, lines 27-34; Obana, paragraphs 0028-0033).

In reference to Claim 10, Schneier and Obana further disclose a chip card (Schneier, column 11, lines 34-44; column 7, lines 38-41; column 12, lines 6-44; Obana, Figure 2, IC card 100).

Claims 11 and 12 are directed to a method corresponding substantially to the module of Claim 1, and are rejected by a similar rationale.

In reference to Claim 13, Schneier discloses a terminal including a data interface that transmits, to a volatile memory in a security module, algorithm code concerning a processing of secrets (column 14, lines 19-21; Figure 4D, volatile memory 23b) and an interface for supplying power such that the volatile memory is cleared if there is an interruption in the power supply (Figure 4D, power 27; column 14, lines 22-26). However, Schneier does not explicitly disclose a power interface for receiving power supplied externally from a terminal, nor does Schneier explicitly disclose that the algorithm code is sent for each communication operation.

Obana discloses a terminal including a data interface that transmits algorithm code to a memory in a security module (Figure 2, IC card 200; paragraphs 0017-0027) and an interface for supplying power (see paragraphs 0017 and 0037) and that the algorithm code is sent for each communication operation (paragraphs 0028-0033). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the security module of Schneier to have an interface for an external supply of power, in order to increase portability by providing the predictable

result of allowing a power supply to be used that is not within the module itself, while still

allowing the memory to be cleared when the power supply is interrupted (see Obana,

paragraph 0037).

Claim 14 is directed to a method corresponding substantially to the terminal of

Claim 13, and is rejected by a similar rationale.

Claim 15 is directed to a method encompassing the performance of the methods

of Claims 11 and 14 simultaneously, and is rejected by a similar rationale. Claim 16

recites limitations corresponding to those recited in Claim 9, and is rejected by a similar

rationale.

Claim 17 is directed to a security module encompassing the limitations of Claims

1 and 8, and is rejected by a similar rationale.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Zachary A. Davis whose telephone number is (571)272-

3870. The examiner can normally be reached on weekdays 8:30-6:00, alternate

Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ZAD/
Examiner, Art Unit 2137

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2137